

A

B

C

D

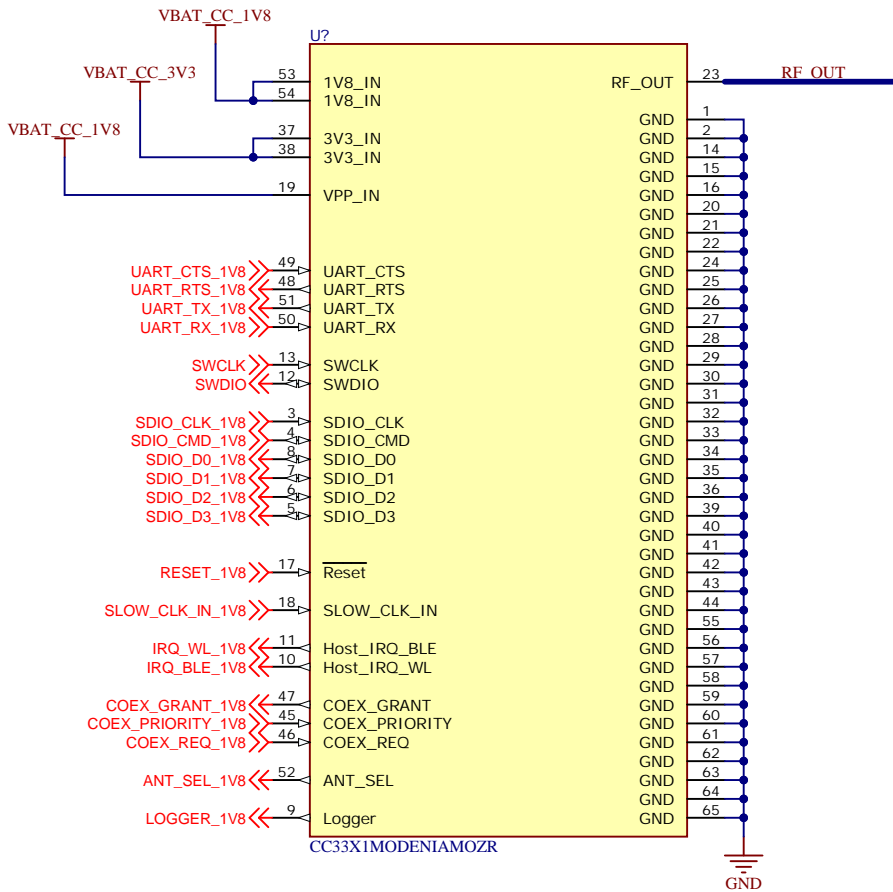
A

B

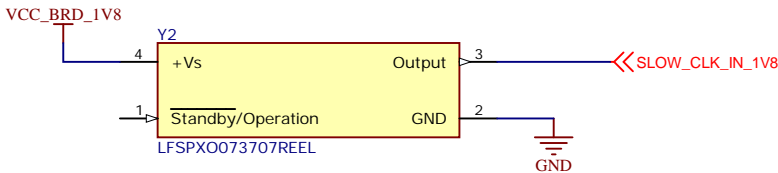
C

D

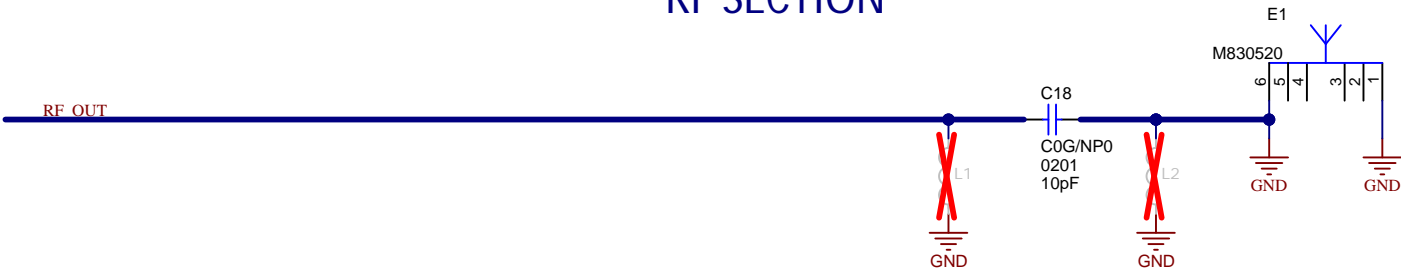
CC33x1MOD TARGET



External Slow Clock (optional)



RF SECTION





PCB Number: MCU135  
PCB Rev: A

PCB  
LOGO  
Texas Instruments

PCB  
LOGO  
FCC disclaimer

PCB  
LOGO  
WEEE logo

PCB  
LOGO  
Texas Instruments

PCB  
LOGO  
ESD Susceptible



SH-J1



Place J12: 2-3

SH-J2



Place J13: 2-3

SH-J3



Place J14: 2-3

SH-J4



Place J6: 1-2

SH-J5



Place J8: 1-2

SH-J6



Place J16: 1-2

SH-J10



Place J15: 1-2

SH-J11



Place J9: 1-2

ZZ1  
Assembly Note  
These assemblies are ESD sensitive, ESD precautions shall be observed.

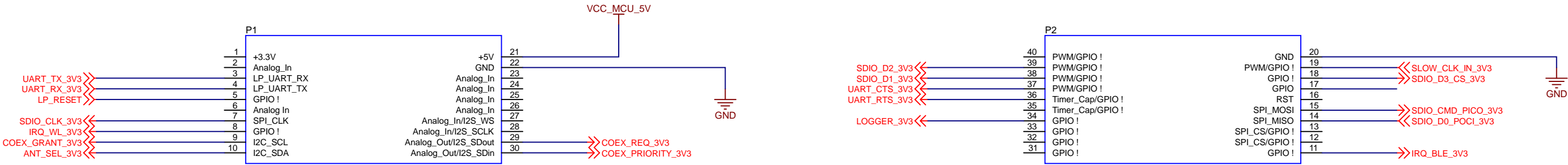
ZZ2  
Assembly Note  
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3  
Assembly Note  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

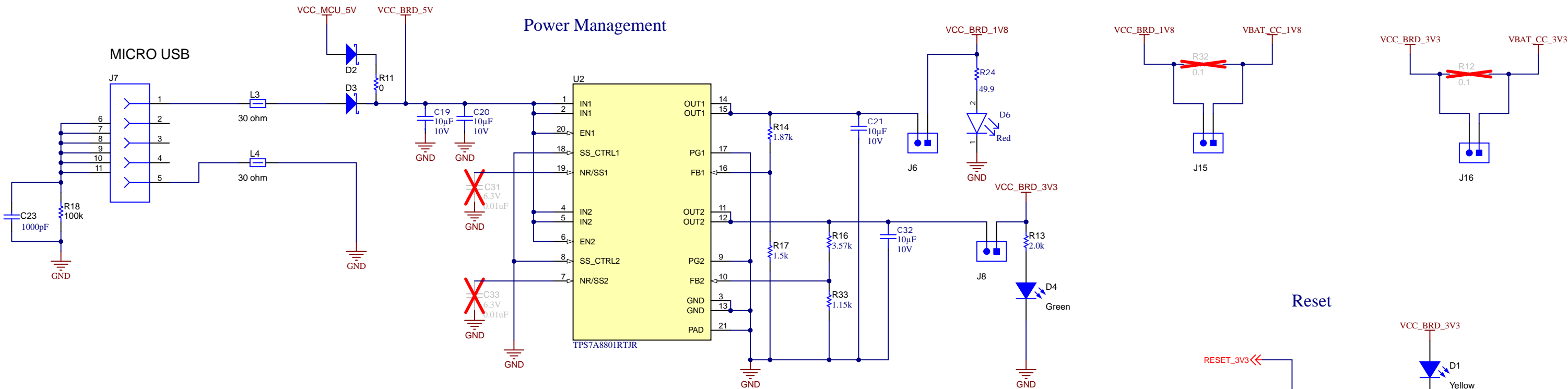
LBL1  
PCB Label  
THT-14-423-10  
Size: 0.65" x 0.20 "

Variant/Label Table	
Variant	Label Text
SB	BP-CC3301MOD
DB	BP-CC3351MOD

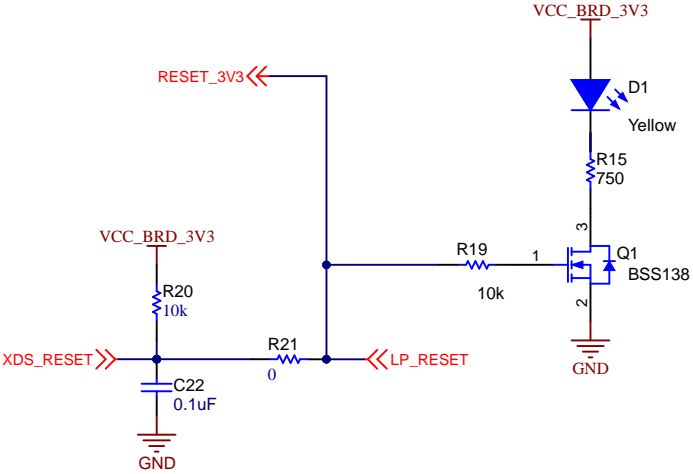
LaunchPad Interface



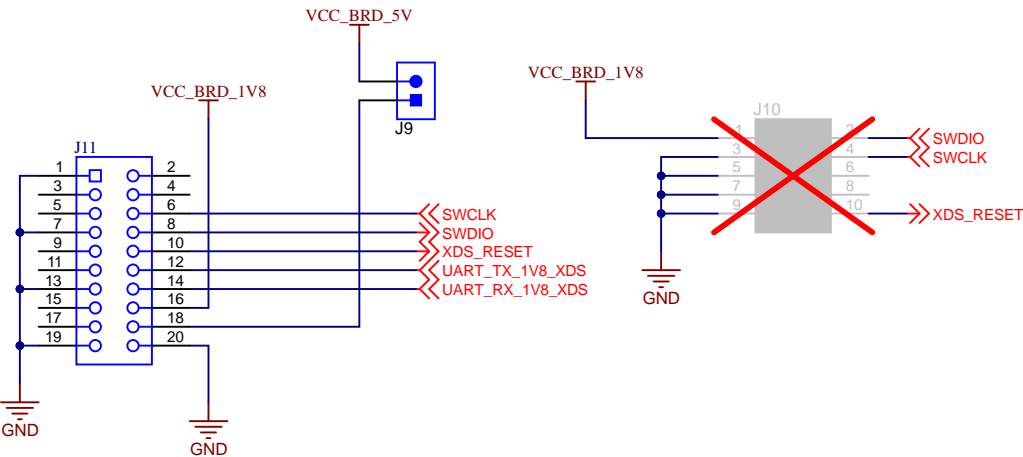
Power Management



Reset



XDS110 Debugger Interface



Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: BP-CC3351MOD	Designed for: Public Release	Mod. Date: 3/10/2025
TID #: N/A	Project Title: BP-CC33xxMOD	
Number: MCU135	Rev: A	Sheet Title:
SVN Rev: b62650c73b7efab593a957ac02519350bb296	File: HostInterface.SchDoc	Sheet: 3 of 4
Drawn By: Jonathan Cohen	Contact: http://www.ti.com/support	Size: B
Engineer: Andy Bui		

Level Shifters

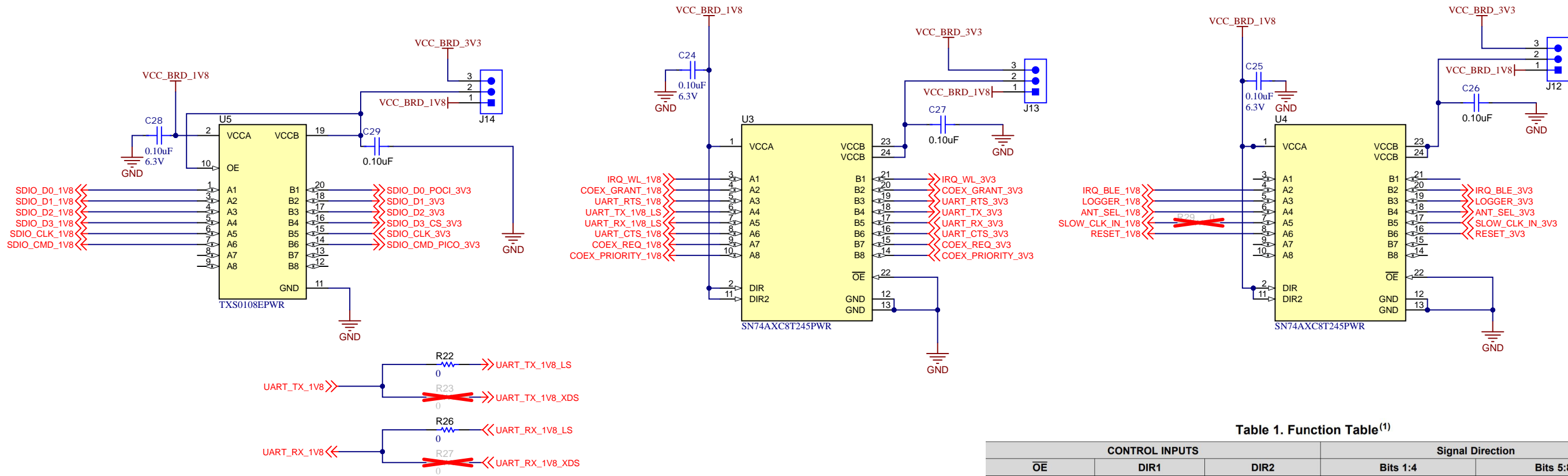


Table 1. Function Table<sup>(1)</sup>

CONTROL INPUTS			Signal Direction	
OE	DIR1	DIR2	Bits 1:4	Bits 5:8
H	X	X	Disabled (Hi-Z)	
L	L	L	B to A	
L	L	H	B to A	A to B
L	H	L	A to B	
L	H	H	A to B	B to A

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.